

**PRINTER RUSH**  
(PTO ASSISTANCE)

1st Request  
QAB

2nd Request

Application : 09/27521

Examiner : Craig

GAU : 2123

From: JEM

Location: (IDC) FMF FDC

Date: 7/11/05

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DOC CODE	DOC DATE	MISCELLANEOUS
<input type="checkbox"/> 1449		<input type="checkbox"/> Continuing Data
<input type="checkbox"/> IDS		<input type="checkbox"/> Foreign Priority
<input type="checkbox"/> CLM		<input type="checkbox"/> Document Legibility
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**[RUSH] MESSAGE:**

Page 1, paragraph 1, line 3. Missing text

Please resolve

Thank you

**[XRUSH] RESPONSE:**

corrected

See Attachment

INITIALS: K

NOTE: This form will be included as part of the official USPTO record, with the Response document coded as XRUSH.

REV 10/04

BEHAVIORAL DIGITAL SIMULATION USING  
HYBRID CONTROL AND DATA FLOW REPRESENTATIONS

Cross Reference to Related Application

5        This application claims priority of provisional U.S. Patent Application No. 60/086,153,  
filed May 19, 1998, entitled "BEHAVIORAL SIMULATION USING A HYBRID CONTROL AND DATA  
FLOW REPRESENTATION" and is related to U.S. Patent Application No. 09/275,687 (Att. Dkt.  
No. ALTRP051), entitled "USING ASSIGNMENT DESIGN NODES WITH CONTROL NODES FOR  
SEQUENTIAL REVIEW DURING BEHAVIORAL SIMULATION" and assigned to the assignee of the  
10    present application, which is hereby incorporated herein by reference for all purposes.

Technical Field of the Invention

15        This invention relates to computer aided design tools and techniques for the interactive  
design, implementation, and simulation of complex circuits and systems and more  
particularly, digital devices, modules, and systems.

Background of the Invention

20        Present computer aided (CAD) systems for the design of electronic circuits, referred to  
as ECAD or electronic CAD systems, assist in the design of electronic circuits by providing a  
user with a set of software tools running on a digital computer. Typically, five major software  
program functions run on the ECAD system, a schematic editor, a compiler, a simulator, a  
verifier, and a layout program. The schematic editor program allows the user of the system to  
enter and/or modify a schematic diagram using the display screen, generating a net list  
(summary of connections between components) in the process. The compiler takes the net list  
as an input, and using a component data base puts all of the information necessary for layout,  
25    verification, and simulation into an object file or files. The verifier checks the schematic for  
design errors, such as multiple outputs connected together, overloaded signal paths, etc. And  
generates error indications if any such design problems exist. The simulator takes the  
schematic object file(s) and simulation models, and generates a set of simulation results,

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